

## **Remarks**

In the Office Action, the Examiner noted that claims 1-13 and 19-39 are pending in the application, and that claims 1-13 and 19-39 are rejected. By this amendment, claims 1, 19, 27, and 39 have been amended. Thus, claims 1-13 and 19-39 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

## ***In the Specification***

In the specification, the table on page 1 has been amended to identify the co-pending applications by their serial numbers, and the Title has been changed, as required by the Examiner.

## ***In the Claims***

### **Rejection Under 35 USC 112 second paragraph**

The Examiner rejected claims 1-13 and 19-39 under 35 U.S.C. § 112, second paragraph, as being indefinite. Applicant has amended claims 1, 19, 27 and 39 to more distinctly claim the subject matter of the invention. In particular, Applicant has amended the claims to make it clear that the two return addresses are compared (claims 1, 27, 39), or provided (claim 19), prior to the return instruction reaching an execution pipeline stage. Applicant respectfully requests the Examiner to withdraw the rejections in view of the claim amendments.

### **Rejection Under 35 USC 102(b)**

The Examiner rejected claims 1-7, 27, 33-35, and 38 under 35 U.S.C. § 102(b), as being anticipated by *Gochman, et al.*, U.S. Patent No. 5,969,868 (hereinafter *Gochman*). Applicant respectfully traverses the rejection of claims 1-7, 27, 33-35, and 38.

With respect to claim 1, Applicant respectfully asserts that *Gochman* does not teach a comparator that compares first and second return addresses prior to a return instruction reaching an execution pipeline stage that finally resolves the return instruction, as recited in amended claim 1. Rather, *Gochman* teaches an execution unit that compares the final

target address with the predicted target address, col. 7, lines 20-21, as the Examiner states in the Office Action. Thus, *Gochman* does not teach comparing two return addresses prior to the return instruction reaching *Gochman*'s execution stage. Therefore, Applicant respectfully asserts that *Gochman* does not anticipate claim 1.

Applicant respectfully asserts *Gochman* does not anticipate or obviate independent claims 27 or 39 for the same reasons discussed above with respect to claim 1.

Applicant respectfully asserts *Gochman* does not anticipate or obviate dependent claims 2-13 and 28-38 because they depend from independent claims 1 and 27, which are not anticipated or obviated by *Gochman* for the reasons discussed above.

### **Rejection Under 35 USC 103**

The Examiner rejected claims 8, 19-26, 28-32, and 39 under 35 U.S.C. § 103, as being unpatentable over *Gochman*. Applicant respectfully traverses the rejection of claims 8, 19-26, 28-32, and 39.

Applicant respectfully asserts *Gochman* does not anticipate or obviate dependent claim 8 because it depends from independent claim 1, which is not anticipated or obviated by *Gochman* for the reasons discussed above.

With respect to claim 19, Applicant respectfully asserts that *Gochman* does not teach first and second call/return stacks that provide first and second return addresses to address selection logic prior to a return instruction reaching an execution pipeline stage that finally resolves return instructions. Rather, *Gochman* teaches an execution unit that pops a final return address off the microprocessor architectural stack, col. 7, lines 7-10, as the Examiner states in the Office Action<sup>1</sup>. Thus, *Gochman* does not teach providing a second

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<sup>1</sup> Applicant still contends as in the response to the first Office Action that when *Gochman* teaches popping the final return address off the microprocessor architectural stack this does not mean popping the final return address off *Gochman*'s Actual Return Stack Buffer, but instead refers to popping the final return address off the architectural stack in memory, which is not a return stack buffer. Therefore, *Gochman* does not teach popping (or providing) a second call/return stack that provides a second return address to address selection logic, or comparing two return addresses provided by two call/return stacks, as recited in the claims. Rather, *Gochman* teaches copying his Actual Return Stack Buffer to his Speculative Return Stack Buffer in response to a branch misprediction, which does not imply popping the final return address off the Actual Return Stack Buffer for provision to address selection logic or for comparing with a first return address. Nevertheless, even if the Examiner is correct in asserting that *Gochman* teaches popping the final return address off the Actual Return Stack Buffer, *Gochman* does not anticipate or obviate Applicant's claims since this is performed in *Gochman*'s execution stage, as discussed above.

return address to address selection logic prior to the return instruction reaching *Gochman*'s execution stage. Therefore, Applicant respectfully asserts that *Gochman* does not anticipate claim 19.

The Examiner rejected claims 9-10 and 36 under 35 U.S.C. § 103, as being unpatentable over *Gochman* in view of *Hilgendorf, et al.*, U.S. Patent No. 5,974,543 (hereinafter *Hilgendorf*). Applicant respectfully traverses the rejection of claims 9-10 and 36.

Applicant respectfully asserts *Gochman* does not anticipate or obviate dependent claims 9-10 and 36 because they depend from independent claims 1 and 19, respectively, which are not anticipated or obviated by *Gochman* for the reasons discussed above.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Applicant earnestly requests the examiner to telephone him at the direct dial number printed below if the examiner has any questions or suggestions concerning the application.

Respectfully submitted,



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By: 